Claims

1. A method for arbitrating across multiple ports, comprising:

assigning a bandwidth limit over a time period to a port associated with a multi-port controller;

receiving data over the port from a requestor;

determining an amount of bandwidth a requestor has previously used;

comparing the amount of bandwidth to the bandwidth limit;

if the amount of bandwidth is greater than the bandwidth limit, then the method includes,

denying access to the port for the period.

2. The method of claim 1, further comprising:

if the amount of bandwidth is less than or equal to the bandwidth limit, then the method includes,

allowing access to the port.

3. The method of claim 1, wherein the method operation of determining an amount of bandwidth a requestor has previously used includes,

determining a number of cycles that commands associated with the port are active over a time period.

4. The method of claim 1, wherein the method operation of comparing the amount of bandwidth to the bandwidth limit includes,

defining a statistics window;

defining a reporting window within the statistics window; and

determining whether active use of the port during the reporting window exceeds the bandwidth limit.

5. The method of claim 4, wherein the statistics window is a period of time that statistics are gathered.

6. The method of claim 4, wherein the reporting window is a time interval that statistics are updated.

7. The method of claim 5, wherein the statistics are bandwidth statistics.

8. The method of claim 1, wherein the method operation of determining an amount of bandwidth a requestor has previously used includes,

incrementing a counter associated with the port when the port is active.

9. A memory controller, comprising:

an initiator block configured to arbitrate requests corresponding to data from multiple ports, the initiator block including,

an arbitration module configured to consider both a latency factor and a bandwidth factor associated with the data from a port to be selected for processing;

a state machine in communication with the arbitration module, the state machine configured to generate a signal to the arbitration module, the signal configured to select the data associated with the port based upon both the latency factor and the bandwidth factor; and

task status and completion circuitry configured to calculate the bandwidth factor based upon previous data selected from the port, the task status and completion circuitry further configured to transmit the calculated bandwidth factor to the state machine.

10. The memory controller of claim 9, wherein the arbitration module includes a multiplexer, the multiplexer configured to select data from one of the multiple ports.

11. The memory controller of claim 9, further comprising:

a placement queue and write data queue block;

a dynamic random access memory (DRAM) command arbitration module; and

a programmable register in communication with the initiator block, the placement queue and write data queue block, and the DRAM command arbitration module.

12. The memory controller of claim 9, wherein the task status and completion circuitry includes,

a queue configured to indicate remaining bandwidth available for a system associated with the memory controller.

13. The memory controller of claim 9, wherein the task status and completion circuitry includes,

an adder associated with each of the multiple ports.

14. The memory controller of claim 13, wherein a width of the adder determines a statistics window and a number of adders associated with the port determines a size of the reporting window.

15. A system, comprising:

a memory controller configured to accommodate a multi-port design, the memory controller including,

an initiator block configured to arbitrate multiple requests for access to the system, the initiator block including,

circuitry configured to define a statistics window; and

circuitry configured to define a reporting window, the reporting window being a segment of the statistics window, wherein the circuitry configured to define a statistics window and the circuitry configured to define a reporting window are further configured to determine a number of cycles that commands for a port are active in the memory controller over a specified number of cycles.

16. The system of claim 15, wherein the statistics window is a period of time that bandwidth statistics are gathered.

17. The system of claim 15, wherein the reporting window is a period of time between an update of bandwidth statistics.

18. The system of claim 15, further comprising:

a programmable register configured to store a bandwidth requirement value and a priority value.

19. The system of claim 18, wherein an output associated with both the circuitry configured to define a statistics window and the circuitry configured to define a reporting window indicates a bandwidth utilization value for the port.

20. The system of claim 19, further comprising:

circuitry configured to compare the bandwidth utilization value with a bandwidth limit value, wherein if the bandwidth utilization value is greater than the bandwidth limit value, access to the port is denied.

21. The system of claim 15, wherein the memory controller is incorporated into a cellular phone.